WHAT IS CLAIMED IS:

1. A display panel drive device comprising:

a parallel-to-serial converter for conducting parallel-to-serial conversion on an input signal and outputting a serial signal;

a transmission section for converting the serial signal output from the parallel-to-serial converter to a signal complying with a differential serial transmission system and transferring a signal via a transmission line;

a reception section for receiving the signal transferred via the transmission line;

a serial-to-parallel converter for conducting serial-to-parallel conversion on the signal received by the reception section and outputting a parallel signal; and

a drive pulse output section for generating a drive pulse to drive a display panel based on the parallel signal output by the serial-to-parallel converter.

2. The display panel drive device according to claim 1, wherein the input signal comprises drive pulse generation control data and a clock.

3. The display panel drive device according to claim 2, comprising:

a display control section for controlling display on a display panel;

a drive section for driving the display panel based on a signal supplied from the display control section; and

a data transfer device for transferring data between the display control section and the drive section,

wherein the data transfer device comprises the parallel-to-serial

converter and the transmission section, and

the drive section comprises the reception section and the serial-to-parallel converter.

4. The display panel drive device according to claim 1, comprising:

a display control section for controlling display on a display panel;

a drive section for driving the display panel based on a signal supplied from the display control section; and

a data transfer device for transferring data between the display control section and the drive section,

wherein the display control section comprises a storage section for storing address data, a readout section for reading out address data stored in the storage section, and a shift clock generation section for generating a shift clock,

the drive section comprises a shift register for successively storing the address data based on the shift clock, a latch circuit for latching the address data stored in the shift register, and a drive circuit for driving the display panel based on the address data output from the latch circuit,

the input signal comprises the address data and the shift clock,

the data transfer device comprises the parallel-to-serial converter and the transmission section, and

the drive section comprises the reception section and the serial-to-parallel converter.

5. The display panel drive device according to claim 1, wherein the input signal comprises the address data and drive pulse generation control data.

6. The display panel drive device according to claim 5, comprising:

a display control section for controlling display on a display panel;

a drive section for driving the display panel based on a signal supplied from the display control section; and

a data transfer device for transferring data between the display control section and the drive section,

wherein the data transfer device comprises the parallel-to-serial converter and the transmission section, and

the drive section comprises the reception section and the serial-to-parallel converter.

7. The display panel drive device according to claim 6,

wherein the display control section comprises a storage section for storing address data, a readout section for reading out address data stored in the storage section, and a control data generation section for generating drive pulse generation control data,

the drive section comprises a shift register for successively storing the address data, a latch circuit for latching the address data stored in the shift register, a drive circuit for driving the display panel based on the address data output from the latch circuit, and a power supply circuit for applying a power supply voltage to the drive circuit based on the drive pulse generation control data.

8. A display panel drive device comprising a display control section for controlling display on a display panel, a drive section for driving the display panel based on a signal supplied from the display control section, and a data

transfer device for transferring data between the display control section and the drive section, wherein

the data transfer device comprises a plurality of transmitters in the display control section, and comprises a plurality of receivers respectively combined with the transmitters and included in the drive section,

each of the transmitters comprises a first PLL circuit for generating a first clock equivalent in frequency to n times an input clock and a second clock equivalent in frequency to the input clock in synchronism with the input clock, a parallel-to-serial converter for conducting parallel-to-serial conversion on drive pulse generation control data based on the first clock output from the first PLL circuit, and a transmission section for converting a serial signal output from the parallel-to-serial converter to a signal complying with a differential serial transmission system and transferring the signal toward the drive section via a transmission line, and

each of the receivers comprises a reception section for receiving the drive pulse generation control data transferred from corresponding one of the transmitters via the transmission line, a second PLL circuit for generating a third clock equivalent in frequency to n times the first clock output and transmitted from the first PLL circuit and a fourth clock equivalent in frequency to the first clock in synchronism with the first clock, and a serial-to-parallel converter for conducting serial-to-parallel conversion on the received drive pulse generation control data based on the third clock output from the second PLL circuit.

9. The display panel drive device according to claim 8, further comprising a clock transmission device for transmitting the input clock as a common clock for the receivers, and a first latch circuit for latching signals

output from the receivers based on the common clock transmitted by the clock transmission device.

10. The display panel drive device according to claim 9, comprising a gate signal transmission device for transmitting a gate signal latched based on the input clock toward the drive section, and a gate circuit for gating a signal latched by the first latch circuit based on the gate signal transmitted by the gate signal transmission device.

11. The display panel drive device according to claim 9, wherein a second latch circuit for latching the drive pulse generation control data based on the input clock is provided before the parallel-to-serial converter, and a third latch circuit for latching a signal output from the serial-to-parallel converter based on the fourth clock is provided between the serial-to-parallel converter and the first latch circuit.

12. The display panel drive device according to claim 8, further comprising a gate signal transmission device for transmitting a gate signal latched based on the input clock toward the drive section, and a gate circuit for gating a signal output from the receivers based on the gate signal transmitted by the gate signal transmission device.

13. The display panel drive device according to claim 12, comprising a clock transmission device for transmitting the input clock as a common clock for the receivers, and a latch circuit for latching a signal output from the gate circuit based on the common clock transmitted by the clock transmission device.

14. A display panel drive device comprising a memory for storing display control data, a readout device for reading out the display control data from the memory based on a first clock having a first frequency, a data transfer device for transferring the display control data read out by the readout device, and a display panel drive section for driving a display panel based on the display control data transferred by the data transfer device,

wherein a clock conversion circuit is provided between the memory and the data transfer device.

15. The display panel drive device according to claim 14,

wherein the clock conversion circuit comprises a FIFO memory, and

the display control data is written into the FIFO memory based on the first clock, and the display control data written into the FIFO memory is read out based on a second clock having a second frequency preset independently of the first clock.

16. The display panel drive device according to claim 15, wherein the data transfer device comprises:

a first PLL circuit for generating a third clock equivalent in frequency to n times the second clock and a fourth clock having the second frequency in synchronism with the second clock;

a parallel-to-serial converter for conducting parallel-to-serial conversion on the display control data based on the third clock output from the first PLL circuit;

a transfer section for converting a serial signal output from the parallel-to-serial converter to a signal complying with a differential serial

transmission system and transferring the signal via a transmission line;

a reception section for receiving the display control data transferred via the transmission line;

a second PLL circuit for generating a fifth clock equivalent in frequency to n times the fourth clock output from the first PLL circuit and transmitted via the transmission line in synchronism with the fourth clock, and a sixth clock equivalent in frequency to the fourth clock; and

a serial-to-parallel converter for conducting serial-to-parallel conversion on the received display control data based on the fifth clock output from the second PLL circuit.

17. A display control device having a display control section of a display panel drive device comprising a display control section for controlling display on a display panel, a drive section for driving the display panel based on a signal supplied from the display control section, and a data transfer device for transferring data between the display control section and the drive section,

wherein the data transfer device comprises in the display control section:

a parallel-to-serial converter for conducting parallel-to-serial conversion on an input signal and outputting a serial signal; and

a transmission section for converting the serial signal output from the parallel-to-serial converter to a signal complying with a differential serial transmission system and transferring a signal toward the drive section via a transmission line, and

the data transfer device comprises in the drive section:

a reception section for receiving the signal transferred via the

transmission line; and

a serial-to-parallel converter for conducting serial-to-parallel conversion on the signal received by the reception section.

18. The display control device according to claim 17, wherein the input signal comprises drive pulse generation control data and a clock.

19. The display control device according to claim 17,

wherein the display control section comprises:

a storage section for storing address data;

a readout section for reading out address data stored in the storage section, and

a shift clock generation section for generating a shift clock,

the drive section comprises a shift register for successively storing the address data based on the shift clock, a latch circuit for latching the address data stored in the shift register, and a drive circuit for driving the display panel based on the address data output from the latch circuit,

the input signal comprises the address data and the shift clock,

the data transfer device comprises the parallel-to-serial converter and the transmission section, and

the drive section comprises the reception section and the serial-to-parallel converter.

20. The display control device according to claim 17, wherein the input signal comprises drive pulse generation control data and a clock.

21. The display control device according to claim 20,

wherein the display control section comprises a storage section for storing address data, a readout section for reading out address data stored in the storage section, and a control data generation section for generating drive pulse generation control data,

the drive section comprises a shift register for successively storing the address data, a latch circuit for latching the address data stored in the shift register, a drive circuit for driving the display panel based on the address data output from the latch circuit, and a power supply circuit for applying a power supply voltage to the drive circuit based on the drive pulse generation control data.

22. A display control device having a display control section of a display panel drive device comprising a display control section for controlling display on a display panel, a drive section for driving the display panel based on a signal supplied from the display control section, and a data transfer device for transferring data between the display control section and the drive section,

wherein the data transfer device comprises a plurality of transmitters in the display control section, and comprises a plurality of receivers respectively combined with the transmitters and included in the drive section,

each of the transmitters comprises a first PLL circuit for generating a first clock equivalent in frequency to n times an input clock and a second clock equivalent in frequency to the input clock in synchronism with the input clock, a parallel-to-serial converter for conducting parallel-to-serial conversion on drive pulse generation control data based on the first clock output from the first PLL circuit, and a transmission section for converting a

serial signal output from the parallel-to-serial converter to a signal complying with a differential serial transmission system and transferring the signal toward the drive section via a transmission line, and

each of the receivers comprises a reception section for receiving the drive pulse generation control data transferred from corresponding one of the transmitters via the transmission line, a second PLL circuit for generating a third clock equivalent in frequency to n times the first clock output and transmitted from the first PLL circuit and a fourth clock equivalent in frequency to the first clock in synchronism with the first clock, and a serial-to-parallel converter for conducting serial-to-parallel conversion on the received drive pulse generation control data based on the third clock output from the second PLL circuit.

23. The display control device according to claim 22, further comprising a clock transmission device for transmitting the input clock as a common clock for the receivers, and a first latch circuit for latching signals output from the receivers based on the common clock transmitted by the clock transmission device.

24. The display control device according to claim 23, comprising a gate signal transmission device for transmitting a gate signal latched based on the input clock toward the drive section, and a gate circuit for gating a signal latched by the first latch circuit based on the gate signal transmitted by the signal transmission device.

25. The display control device according to claim 23, wherein a second latch circuit for latching the drive pulse generation control data based on the

input clock is provided before the parallel-to-serial converter, and a third latch circuit for latching a signal output from the serial-to-parallel converter based on the fourth clock is provided between the serial-to-parallel converter and the first latch circuit.

26. The display control device according to claim 22, further comprising a gate signal transmission device for transmitting a gate signal latched based on the input clock toward the drive section, and a gate circuit for gating a signal output from the receivers based on the gate signal transmitted by the gate signal transmission device.

27. The display control device according to claim 26, comprising a clock transmission device for transmitting the input clock as a common clock for the receivers, and a latch circuit for latching a signal output from the gate circuit based on the common clock transmitted by the clock transmission device.

28. A drive device having a drive section of a display panel drive device comprising a display control section for controlling display on a display panel, a drive section for driving the display panel based on a signal supplied from the display control section, and a data transfer device for transferring data between the display control section and the drive section,

wherein the data transfer device comprises in the display control section:

a parallel-to-serial converter for conducting parallel-to-serial conversion on an input signal and outputting a serial signal; and

a transmission section for converting the serial signal output from

the parallel-to-serial converter to a signal complying with a differential serial transmission system and transferring a signal toward the drive section via a transmission line, and

the drive section comprises:

a reception section for receiving the signal transferred via the transmission line; and

a serial-to-parallel converter for conducting serial-to-parallel conversion on the signal received by the reception section.

29. The drive device according to claim 28, wherein the input signal comprises drive pulse generation control data and a clock.

30. The drive device according to claim 28, wherein

the display control section comprises a storage section for storing address data, a readout section for reading out address data stored in the storage section, and a shift clock generation section for generating a shift clock,

the drive section comprises a shift register for successively storing the address data based on the shift clock, a latch circuit for latching the address data stored in the shift register, and a drive circuit for driving the display panel based on the address data output from the latch circuit,

the input signal comprises the address data and the shift clock,

the data transfer device comprises the parallel-to-serial converter and the transmission section, and

the drive section comprises the reception section and the serial-to-parallel converter.

31. The drive device according to claim 28, wherein the input signal comprises drive pulse generation control data and a clock.

32. The drive device according to claim 31, wherein

the display control section comprises a storage section for storing address data, a readout section for reading out address data stored in the storage section, and a control data generation section for generating drive pulse generation control data,

the drive section comprises a shift register for successively storing the address data, a latch circuit for latching the address data stored in the shift register, a drive circuit for driving the display panel based on the address data output from the latch circuit, and a power supply circuit for applying a power supply voltage to the drive circuit based on the drive pulse generation control data.

33. A drive device having a drive section of a display panel drive device comprising a display control section for controlling display on a display panel, a drive section for driving the display panel based on a signal supplied from the display control section, and a data transfer device for transferring data between the display control section and the drive section,

wherein the data transfer device comprises a plurality of transmitters in the display control section, and comprises a plurality of receivers respectively combined with the transmitters and included in the drive section,

each of the transmitters comprises a first PLL circuit for generating a first clock equivalent in frequency to n times an input clock and a second clock equivalent in frequency to the input clock in synchronism with the

input clock, a parallel-to-serial converter for conducting parallel-to-serial conversion on drive pulse generation control data based on the first clock output from the first PLL circuit, and a transmission section for converting a serial signal output from the parallel-to-serial converter to a signal complying with a differential serial transmission system and transferring the signal toward the drive section via a transmission line, and

each of the receivers comprises a reception section for receiving the drive pulse generation control data transferred from corresponding one of the transmitters via the transmission line, a second PLL circuit for generating a third clock equivalent in frequency to n times the first clock output and transmitted from the first PLL circuit and a fourth clock equivalent in frequency to the first clock in synchronism with the first clock, and a serial-to-parallel converter for conducting serial-to-parallel conversion on the received drive pulse generation control data based on the third clock output from the second PLL circuit.

34. The drive device according to claim 33, further comprising a clock transmission device for transmitting the input clock as a common clock for the receivers, and a first latch circuit for latching signals output from the receivers based on the common clock transmitted by the clock transmission device.

35. The drive device according to claim 34, comprising a gate signal transmission device for transmitting a gate signal latched based on the input clock toward the drive section, and a gate circuit for gating a signal latched by the first latch circuit based on the gate signal transmitted by the gate signal transmission device.

36. The drive device according to claim 34, wherein a second latch circuit for latching the drive pulse generation control data based on the input clock is provided before the parallel-to-serial converter, and a third latch circuit for latching a signal output from the serial-to-parallel converter based on the fourth clock is provided between the serial-to-parallel converter and the first latch circuit.

37. The drive device according to claim 33, further comprising a gate signal transmission device for transmitting a gate signal latched based on the input clock toward the drive section, and a gate circuit for gating a signal output from the receivers based on the gate signal transmitted by the gate signal transmission device.

38. The drive device according to claim 37, comprising a clock transmission device for transmitting the input clock as a common clock for the receivers, and a latch circuit for latching a signal output from the gate circuit based on the common clock transmitted by the clock transmission device.

39. A data transfer system for conducting data transfer between a first device and a second device,

wherein the first device comprises a plurality of transmitters, and the second device comprises a plurality of receivers respectively combined with the transmitters,

each of the transmitters comprises a first PLL circuit for generating a first clock equivalent in frequency to n times an input clock and a second

clock equivalent in frequency to the input clock in synchronism with the input clock, a parallel-to-serial converter for conducting parallel-to-serial conversion on data based on the first clock output from the first PLL circuit, and a transmission section for converting a serial signal output from the parallel-to-serial converter to a signal complying with a differential serial transmission system and transferring the signal toward the second device via a transmission line, and

each of the receivers comprises a reception section for receiving the data transferred from corresponding one of the transmitters via the transmission line, a second PLL circuit for generating a third clock equivalent in frequency to n times the first clock output and transmitted from the first PLL circuit and a fourth clock equivalent in frequency to the first clock in synchronism with the first clock, and a serial-to-parallel converter for conducting serial-to-parallel conversion on the received data based on the third clock output from the second PLL circuit.

40. The data transfer system according to claim 39, comprising a clock transmission device for transmitting the input clock as a common clock for the receivers, and a first latch circuit for latching signals output from the receivers based on the common clock transmitted by the clock transmission device.

41. The data transfer system according to claim 40, comprising a gate signal transmission device for transmitting a gate signal latched based on the input clock toward the second device, and a gate circuit for gating a signal latched by the first latch circuit based on the gate signal transmitted by the gate signal transmission device.

42. The data transfer system according to claim 40, wherein a second latch circuit for latching the data based on the input clock is provided before the parallel-to-serial converter, and a third latch circuit for latching a signal output from the serial-to-parallel converter based on the fourth clock is provided between the serial-to-parallel converter and the first latch circuit.

43. The data transfer system according to claim 39, further comprising a gate signal transmission device for transmitting a gate signal latched based on the input clock toward the second device, and a gate circuit for gating a signal output from the receivers based on the gate signal transmitted by the gate signal transmission device.

44. The data transfer system according to claim 43, comprising a clock transmission device for transmitting the input clock as a common clock for the receivers, and a latch circuit for latching a signal output from the gate circuit based on the common clock transmitted by the clock transmission device.

45. A data transmission device having a first device comprising a data transfer system for conducting data transfer between a first device and a second device,

wherein the first device comprises a plurality of transmitters, and the second device comprises a plurality of receivers respectively combined with the transmitters,

each of the transmitters comprises a first PLL circuit for generating a first clock equivalent in frequency to n times an input clock and a second

clock equivalent in frequency to the input clock in synchronism with the input clock, a parallel-to-serial converter for conducting parallel-to-serial conversion on data based on the first clock output from the first PLL circuit, and a transmission section for converting a serial signal output from the parallel-to-serial converter to a signal complying with a differential serial transmission system and transferring the signal toward the second device via a transmission line, and

each of the receivers comprises a reception section for receiving the data transferred from corresponding one of the transmitters via the transmission line, a second PLL circuit for generating a third clock equivalent in frequency to n times the first clock output and transmitted from the first PLL circuit and a fourth clock equivalent in frequency to the first clock in synchronism with the first clock, and a serial-to-parallel converter for conducting serial-to-parallel conversion on the received data based on the third clock output from the second PLL circuit.

46. The data transmission device according to claim 45, wherein the data transfer system comprises a clock transmission device for transmitting the input clock as a common clock for the receivers, and a first latch circuit for latching signals output from the receivers based on the common clock transmitted by the clock transmission device.

47. The data transmission device according to claim 46, wherein the data transfer system comprises a gate signal transmission device for transmitting a gate signal latched based on the input clock toward the second device, and a gate circuit for gating a signal latched by the first latch circuit based on the gate signal transmitted by the gate signal transmission

device.

48. The data transmission device according to claim 46, wherein a second latch circuit for latching the data based on the input clock is provided before the parallel-to-serial converter, and a third latch circuit for latching a signal output from the serial-to-parallel converter based on the fourth clock is provided between the serial-to-parallel converter and the first latch circuit.

49. The data transmission device according to claim 45, wherein the data transfer system comprises a gate signal transmission device for transmitting a gate signal latched based on the input clock toward the second device, and a gate circuit for gating a signal output from the receivers based on the gate signal transmitted by the gate signal transmission device.

50. The data transmission device according to claim 49, wherein the data transfer system comprises a clock transmission device for transmitting the input clock as a common clock for the receivers, and a latch circuit for latching a signal output from the gate circuit based on the common clock transmitted by the clock transmission device.

51. A data reception device having a second device comprising a data transfer system for conducting data transfer between a first device and a second device,

wherein the first device comprises a plurality of transmitters, and the second device comprises a plurality of receivers respectively combined with the transmitters,

each of the transmitters comprises a first PLL circuit for generating a first clock equivalent in frequency to n times an input clock and a second clock equivalent in frequency to the input clock in synchronism with the input clock, a parallel-to-serial converter for conducting parallel-to-serial conversion on data based on the first clock output from the first PLL circuit, and a transmission section for converting a serial signal output from the parallel-to-serial converter to a signal complying with a differential serial transmission system and transferring the signal toward the second device via a transmission line, and

each of the receivers comprises a reception section for receiving the data transferred from corresponding one of the transmitters via the transmission line, a second PLL circuit for generating a third clock equivalent in frequency to n times the first clock output and transmitted from the first PLL circuit and a fourth clock equivalent in frequency to the first clock in synchronism with the first clock, and a serial-to-parallel converter for conducting serial-to-parallel conversion on the received data based on the third clock output from the second PLL circuit.

52. The data reception device according to claim 51, wherein the data transfer system comprises a clock transmission device for transmitting the input clock as a common clock for the receivers, and a first latch circuit for latching signals output from the receivers based on the common clock transmitted by the clock transmission device.

53. The data reception device according to claim 52, wherein the data transfer system comprises a gate signal transmission device for transmitting a gate signal latched based on the input clock toward the second device, and

a gate circuit for gating a signal latched by the first latch circuit based on the gate signal transmitted by the gate signal transmission device.

54. The data reception device according to claim 52, wherein a second latch circuit for latching the data based on the input clock is provided before the parallel-to-serial converter, and a third latch circuit for latching a signal output from the serial-to-parallel converter based on the fourth clock is provided between the serial-to-parallel converter and the first latch circuit.

55. The data reception device according to claim 51, wherein the data transfer system comprises a gate signal transmission device for transmitting a gate signal latched based on the input clock toward the second device, and a gate circuit for gating a signal output from the receivers based on the gate signal transmitted by the gate signal transmission device.

56. The data reception device according to claim 55, wherein the data transfer system comprises a clock transmission device for transmitting the input clock as a common clock for the receivers, and a latch circuit for latching a signal output from the gate circuit based on the common clock transmitted by the clock transmission device.